INTEGRATED CIRCUIT HAVING MULTIPLE MEMORY TYPES AND METHOD OF FORMATION

Abstract of the Disclosure

A transistor (10) is formed having three separately controllable gates (44, 42, 18). The three gate regions may be electrically biased differently and the gate regions may have different conductivity properties. The dielectrics on the channel sidewall may be different than the dielectrics on the top of the channel. Electrical contacts to source, drain and the three gates is selectively made. By including charge storage layers, such as nanoclusters, adjacent the transistor channel and controlling the charge storage layers via the three gate regions, both volatile and non-volatile memory cells are realized using the same process to create a universal memory process. When implemented as a volatile cell, the height of the transistor and the characteristics of channel sidewall dielectrics control the memory retention characteristics. When implemented as a nonvolatile cell, the width of the transistor and the characteristics of the overlying channel dielectrics control the memory retention characteristics.